WHAT IS CLAIMED IS:

1. An electronic sub assembly comprising a circuitized laminated substrate having top and bottom surfaces, and at least one edge surface between said top and bottom surfaces, one or more active or passive devices mounted on at least one of the top and bottom surfaces, a conductive lead embedded in the substrate electrically connected to an active or passive device mounted on said at least one edge surface, the conductive lead also electrically connected to at least one device on the top or bottom surface.

2. The sub assembly according to claim 1 wherein each of the active or passive devices is selected from the group including chips, diodes, resistors, capacitors and printed wiring boards.

3. The sub assembly according to claim 1 further including an electrically conductive via extending into the substrate from each device on the top or bottom surface into contact with a conductive lead connected to an edge mounted device.

4. The sub assembly according to claim 1 wherein the laminated substrate is selected from the group comprising a single or multiple laminates of a fiberglass reinforced prepreg and a conductive layer, and a single or multiple laminates of a ceramic module and a conductive layer.

5. A method of making an electronic sub assembly comprising fabricating a circuitized laminated substrate having top and bottom surfaces and an edge surface between said top and bottom surfaces, providing one or more active or passive devices mounted on at least one of the top and bottom surfaces, mounting an active or a

passive device on said edge surface, embedding a conductive lead in the substrate, electrically connecting said conductive lead to said at least one active or passive device mounted on said edge surface, and electrically connecting the conductive lead to the at least one device on said top or bottom surface of the substrate.

6. The method according to claim 5 including the further step of providing a via to connect each device mounted on the top or bottom surface to a conductive lead in the substrate leading to a device on said edge surface.

7. The method according to claim 5 wherein said edge surface is sheared to expose a plurality of connection points at the end of each conductive lead, each connection point providing means for the conductive lead to be joined to an active or passive devices mounted on said edge surface.

8. A printed circuit board having two spaced apart, generally parallel surfaces comprising a top surface and a bottom surface, an edge surface between said top and bottom surfaces, a plurality of conductive leads embedded in the circuit board parallel to the top and bottom surfaces and terminating in one or more connection points along the edge surface, an active or passive device mounted on said edge surface and electrically joined through at least one of said connection points to at least one of the conductive leads, and at least one active or passive device mounted on the top or bottom surface electrically joined to the edge mounted device.

9. The printed circuit board according to claim 8 further including a via on the top or bottom surface, and coupled to a top or bottom mounted device, said via

extending into the substrate into contact with a conductive lead connected to said edge mounted device.

10. The printed circuit board according to claim 8 wherein each active or passive device is selected from the group including chips, diodes, resistors, capacitors and printed wiring boards.

11. A method of increasing the proximity of active or passive devices on a circuitized laminated substrate comprising:

a) providing the substrate with top and bottom generally parallel surfaces and an edge surface therebetween;

b) embedding a plurality of conductive leads in the laminated substrate parallel to the top and bottom surfaces, at least one end of each lead terminating at said edge surface;

c) mounting an active or passive device on the top or bottom surface;

d) providing at least one via extending from the top and/or the bottom planar surface into the substrate for the attachment of said mounted device to at least one of the conductive leads;

e) attaching at least one active or passive device on said edge surface, and

f) providing a plurality of connection points on said edge surface for the attachment of an edge surface mounted active or passive device through at least one conductive lead and via to a top or bottom mounted device.

12. The method according to claim 11 wherein each of the active or passive devices is selected from the group including chips, diodes, resistors, capacitors and printed wiring boards.

13. The method according to claim 11 wherein the substrate is selected from the group consisting of a printed circuit board and a ceramic module.

14. A device comprising a multi-layered circuitized sub assembly, and a semiconductor chip, the sub assembly having two substantially parallel surfaces and an edge surface between the two surfaces, at least one conductive lead embedded in the sub assembly between the surfaces, one end of the at least one conductive lead terminating in electrical connection points on said edge surface, the semiconductor chip containing contacts electrically connected to the connection points on said edge of the sub assembly, and at least one active or passive device mounted on one of the generally parallel surfaces of the sub assembly in electrical contact with said at least one conductive lead.

15. The device according to claim 14 wherein the semiconductor chip is an optical chip.

16. The device according to claim 15 wherein the connection points terminate in contact pads on said edge surface of the sub assembly, and the optical chip is coupled to the contact pads.

17. The device according to claim 16 wherein the optical chip is coupled to the contact pads through solder ball connectors.

18. The device according to claim 14 wherein the sub assembly comprises a plurality of laminates forming a stack, all of the laminates in the stack having coplanar edge surfaces having the electrical connection points, and a stepped edge surface whereby each successive laminate in the stack is shorter than the laminate immediately there beneath, thereby forming an exposed planar surface on the lower laminate, the device further including an active or passive device mounted on at least some of the exposed planar surfaces.

19. The device according to claim 18 wherein one or more of the active or passive devices on the generally parallel surfaces of the sub assembly are plug-in connectors to permit the device to interface with a computer.

20. The device according to claim 19 further including one or more vias extending from each exposed planar surface of a laminate into contact with a conductive lead to provide a connection between the semiconductor chip and a connector.

21. The device according to claim 18 wherein the coplanar edge of the stack of laminates forms an angle of 90° with respect to the planar surfaces of the laminates.

22. The device according to claim 18 wherein the coplanar edge of the stack of laminates forms an angle less than 90° with respect to the planar surfaces of the laminates.

23. The device according to claim 15 further including an optical interface between the optical chip and a laser wafer.

24. The device according to claim 23 wherein the interface comprises an optically transparent epoxy resin.

25. The device according to claim 22 wherein the laser wafer includes transmitters to transmit optical data through optical receivers on the optical chip to the sub assembly.

26. The device according to claim 25 wherein the laser wafer is a vertical cavity surface emitting laser.